Novel HW/SW Design Methodologies for Ad-Hoc Sensor Networks in Future Applications

A.K. Chandra-Sekaran
Institut für Technik der Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: ashok@itiv.uka.de

K. Paulsson
Institut für Technik der Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: paulsson@itiv.uka.de

J. Becker
Institut für Technik der Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: becker@itiv.uka.de

O. Sander
Institut für Technik der
Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: sander@itiv.uka.de

M. Hübner
Institut für Technik der
Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: huebner@itiv.uka.de

K. Müller-Glaser
Institut für Technik der
Informationsverarbeitung
Universität Karlsruhe
Karlsruhe, Germany
e-mail: kmg@itiv.uka.de

Abstract[1]

Sensor networks play an important role in actual and future everyday applications. Mobile community and the requirements to supply people as well as electronic systems with information from their environment is a challenging task. Networking in the form of information transfer has to be supported by novel sensors, computing-systems and intelligent mechanisms to process the flood of data with high efficiency. In this paper we investigate into the energy efficient techniques, novel high adaptive and run-time reconfigurable hardware-architectures and high level algorithms dealing with the methodologies these techniques provide.

1. Introduction

Since a long time sensor networks play an important role in academic and industrial research. The introduction of mobile technologies like cell-phones and PDAs brought the communication technologies in nearly everyone's home. Since then, the investigation in power aware and high performance hardware had a new focus for researchers and designers. The progress in hardware, communication technologies and the corresponding methods open a wide area for new methodologies and certainly a revision of existing paradigms which may have now another impact for future systems and applications.

With the term ad-hoc sensor network always come the ideas of flexibility, reactivity, adaptivity and autonomy. To provide all these features also the hardware of the sensor nodes must be adaptive. Novel hardware-reconfigurable architectures enable to adapt to external and internal requirements. Those could be the power situation (capacity of battery), computation performance or changing algorithms for communication and data processing. By using hardware-reconfigurable architectures it is possible to exploit real parallelism by running a maximum number of tasks on the chip's area. This increased data-processing performance does not only has its benefit in computation power, additionally the clock speed of the system can be reduces by keeping the required real-time conditions which were essential for

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a variety of applications. This leads to reduced power consumption by simultaneously increasing of computing resources. By facing the possibility of run-time reconfiguration another aspect for reducing the power consumption is coming up. By outsourcing of parts of architecture to external memory, the chip size can be reduced and therefore the static power can additionally be decreased.

The progress in reconfigurable architectures regarding their energy consumption but also in novel designs with integrated analogue parts, close the gap to traditional microcontrollers more and more. Exploiting run-time reconfiguration and intelligent methods for scheduling tasks and run-time power and performance optimization, will definitely lead to an alternative architecture and partly a substitution of microcontrollers.

The paper is organized in the following manner: chapter 2 describes one possible application for a wireless sensor network and in chapter 3 the mote which has been specifically developed for this application and its power consumption results are presented. Section 4 discuss how more flexibility can be integrated in the hardware architectures of sensor nodes by exploiting reconfigurable hardware, and section 5 further extends this discussion by describing some of the main challenges of future sensor network applications and what can be done to meet the increasing requirements. Finally, section 6 concludes the paper.

2. Application for WSN

WSN are perceived as dynamic, ad-hoc networks. As opposed with standard networks, where topology is barely changing, the WSN have to deal in most of the application scenarios with an undefined network topology. The nodes have to form ad-hoc networks and organize themselves in order to communicate and process the data. In this paper we consider on of the potential application for such a WSN: - Health care. Some of the Health care scenarios based on wireless sensor networking are:

- Assisted living-Health smart home
- Hospital network
- Body Area Network (Personal health monitoring)
- Disaster management

The main challenges in WSN for health cared based applications are as follows:

- "Wireless monitoring" includes physiological monitoring of parameters (such as heart rate, blood pressure, blood oximetry) and physical activity monitoring (such as monitoring of movement, fall detection, location tracking, gastrointestinal telemetry, and other physical activities). Due to wireless monitoring the sensor devices employed in hospitals will increase drastically. The large number of medical sensor nodes in these wireless hospital sensor network should be easily integrated to form ad-hoc network and provide flexibility leading to "health care-on-demand" [6].
- The real-time constraints have to be met especially during emergency conditions.
- The sensor nodes should provide user comfort to the patients. Thus the sensor nodes should be miniaturised and have a long battery life time.
- Due to miniscule size of the medical sensor node its computational resources are restricted. Therefore the sensor node computation and inter-nodal communication should be compliant with the energy efficient techniques.

3. Energy Efficiency Techniques for Health Care Based WSN

A power aware design methodology emphasizes the graceful scalability of energy consumption with factors such as available resources, event frequency and desired output quality at all levels of the system hierarchy. The architecture for a power-aware sensor node highlights the collaboration between software that is capable of energy-quality trade-offs and hardware with scalable energy consumption [7]. Scalability is an important factor since it allows the user to implement operational policy which often varies significantly over the lifetime of the system.

A power aware design is to be used for the sensor nodes of the health care based applications. Dynamic voltage scaling (DVS) on the sensor node processor enables energy saving from the scalable algorithms that run on the node. Dynamic voltage scaling can be setup using the commercial processor, digital DC-DC converter and power aware operating system of the sensor node. DVS exploits variability in processor workload and latency constraints and realizes the energy quality trade-of at the circuit level. Duty cycling can be introduced such that the power aware sensor node enables its embedded operating system to make transitions to different sleep states based on observed event statistics.

Because of the unique attenuation characteristics of radio-frequency (RF) signals, a multihop RF network provides a significant energy saving over a single hop network for the same distance [8].

In the recent years wireless technologies like WLAN and Zigbee have emerged in the mobile health services. The new short range, low power, low rate wireless networking Zigbee standard (IEEE 802.15.4 based) complements the high data rate technologies such as WLAN and open the door for many new applications. It has been developed as a low data rate solution with multi-month to multiyear battery life and very low complexity. This standard operates at two bands, the 2.4 GHz band with a maximum rate of 250 kbps and the 868-928 MHz band with data rates between 20 and 40 kbps.

As a primitive model of the power aware Zigbee sensor nodes to be used in the health care applications, a Zigbee compliant mote called ZigTiv which runs the IEEE 802.15.4 MAC software is developed. The following section describes about the ZigTiv mote.

3.1. Zigbee Compliant Mote – ZIGTIV

ZigTiv mote is a processor-radio board which comprises of the Texas Instrumentation MSP430 microcontroller connected to the Chipcon CC2420 2.4 GHz transceiver through SPI (Synchronous peripheral Interface) as shown in Figure 1.

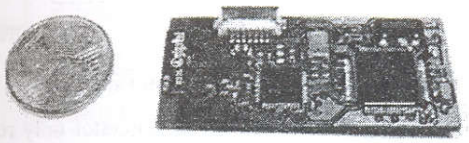

Figure 1. ZigTiv Mote

Microcontroller

MSP430 is an ultra low power 16-bit RISC processor architecture with extended battery life. Zigtiv uses the MSP430 family member F1611 having 48kB flash, 128 Byte information storage and 10 kB RAM [9]. The Internal digitally controlled oscillator (DCO) with RC-type characteristics is used as clock source for CPU and can attain up to 8 MHz clock frequency. ZigTiv is operated with the frequency of 4.1 MHz at 2.1V voltage supply. For optimal low-power performance, the MSP430 can be configured to oscillate with a low-power 32,786-Hz watch crystal, providing a stable time base for the system and low power stand-by operation. There are five power saving modes available and the wakeup time from standby mode is less than 6 us. In Low Power Mode3 the CPU, DCO oscillator and DC generator are disabled and the clock source with 32,786-Hz watch crystal is active. The most important factor for reducing power consumption is using the MSP430's clock system to maximize the time in Low Power Mode3 (LPM3).

Transceiver

In ZigTiv the 2.4 GHz IEEE 802.15.4 compliant RF transceiver of Chipcon CC2420 designed for low power and low voltage wireless applications is utilized [10]. CC2420 includes a digital direct sequence spread spectrum base band modem with 2 MChips/s and 250 kbps effective data rate. It is suitable for both RFD and FFD operation. The CC2420 provides a digital received signal strength indicator (RSSI) that may be read any time.

Antenna

The Rufa SMD 2.4 GHz quarter wave type antenna [11] from GigaAnt is chosen for ZigTiv. Rufa provides a higher bandwidth of 180 MHz, thus making it less sensitive to surroundings and changes to applications.

IEEE 802.15.4 Mac Software Layer

The Chipcon IEEE 802.15.4 MAC and PHY software implements the functionality as specified by the IEEE 802.15.4 specifications [12]. This software is available from Chipcon under a licensing agreement. Based on the C implementation of this software written for Atmel AVR microcontroller, the MAC was developed for the MSP430 microcontroller which is used in ZigTiv.

ZigTiv Power Consumption

The power consumption measurements of the ZigTiv mote running the MSP430 MAC layer is as shown in Table 1. The current consumption measurements of ZigTiv in various modes-MCU active + Tx/Rx mode, LPM 3 suggest that ZigTiv has reduced power consumption and is a positive step in the direction of development of an power aware Zigbee health monitoring sensor nodes for health care applications.

4. Advanced Sensor Nodes Based on Reconfigurable Hardware

4.1. Overview

Traditionally, the tasks of a sensor node are relatively simple. The nodes are optimized for collection of data, simple data processing and limited communication. During the last years however, the requirements of sensor networks have increased for many applications. Therefore new research areas such as Organic Computing [4] are now investigating the design of self-organizing sensor networks. Self-organizing sensor networks have characteristics such as self-healing, self-optimization and self-configuration.

Table 1. Power Consumption of ZigTiv Mote

Operation	ZigTiv Mote
MCU Frequency	4.1 MHz @ 2.15 V
MCU Active(DCO on)	1.15 mA
MCU LPM3	< 2uA
MCU Active + TX @0 dbm	19.6 mA
MCU Active + RX	21.7 mA
MCU Wakeup Time	6 us
Minimum Voltage	2.1 V
Maximum Voltage	3.6V

These additional requirements of sensor networks further increase the demands of the hardware architectures. For more computational power while maintaining a low power consumption alternative hardware such as FPGAs must be investigated for usage in sensor networks instead of traditional microcontrollers. FPGAs allow the computation of several tasks in parallel and some of these architectures, such as Xilinx FPGAs, also allow dynamic and partial hardware reconfiguration.

4.2. Failure Detection and Fault Tolerance

Methods for detecting failures on reconfigurable hardware and recover from them have been investigated in earlier work described in [1]. There, dynamic reconfigurable test benches and Dynamic Triple Module

redundancy has been implemented and tested in a dynamic and partial hardware reconfigurable system for automotive applications. To integrate Build- In- Self-Test, BIST, in embedded systems is a standard method for detecting failures during run-time, and has been further optimized in [1] by configuring the test bench only when tests are required during run-time. This way, the problem with hardware overhead due to the test circuit itself is prohibited.

This kind of test method can detect so called soft errors such as bit flips caused by Single Event Upsets.

Dynamic Triple Module Redundancy, DTMR, has also been investigated for detecting hardware failures [1]. Triple Module Redundancy, TMR, is traditionally used in many applications that require a high safety, and of course this method increases the hardware overhead. In systems based on reconfigurable architectures, the hardware overhead can be avoided by only configuring two copies of the function under test whenever tests are required or whenever tests can be performed without disturbing the system functionality, which is described further in [1].

4.3. Power Optimized System Integration

FPGAs also have the advantage that they offer a simplified design process. Functions can be integrated in the systems as IP cores in a high level design environment, together with other components such as soft-core microcontrollers and required peripherals. Some tasks such as control tasks are optimized to be executed in software, which is why FPGA vendors provide soft-core microcontrollers for FPGA [5].

A designer can also define custom VHDL cores for FPGAs. For example, digital parts of AD/DA converters can be integrated on FPGAs. Such components are standard components on sensor nodes, but normally implemented as external components or as microcontroller peripherals. By reducing the number of external components costs can be reduced as well as a simplified design process can be achieved. If reconfiguration is exploited to configure the components whenever they are required, it would also reduce the chip area compared to if they are constantly configured. This would also reduce the static power consumption.

Xilinx [2] offers delta-sigma DA and AD converters as IP cores. They are small cores and very usable in audio applications. Unfortunately they do not provide a high performance, according to the specifications. However, real tests of the delta-sigma DA converter show that they can be used even in applications requiring a higher performance. The specific application which was used for the tests was the digital generation of a sinus signal. Digital sinus values are read out from a block-RAM on FPGA and converted into and analogue signal by a DA-converter. In the first implementation of the digital sinus generator an external DA-converter was used, and then the DA-converter was integrated on FPGA by using the Xilinx delta-sigma converter. In order to improve the performance of the DA-converter, the interface to the On-Chip Peripheral Bus, OPB, on the converter was removed and the component was directly attached to the output of the block-RAM. See Figure 3 for a structural overview of the sinus generator.

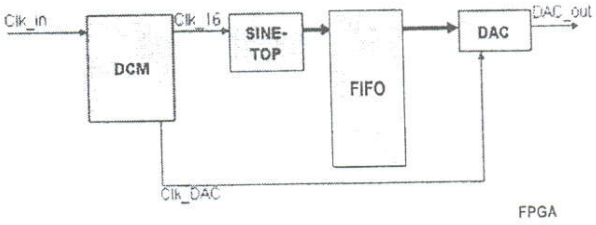

Figure 3. Sinus Generator

This implementation of the sinus generator only requires an external low pass filter for generating an analogue signal, in combination with an anti-alias filter for eliminating high-frequency components. The anti-alias filter was required even with the external DA-converter, so in practice the external DA-converter has been reduced to an external low pass filter. The digital DA-converter must only be configured whenever required.

Figure 4 shows the signal spectrum of the generated sinus signal, without filtering the signal through an anti-alias filter. As can be seen, the sinus generates clearly separateed frequency peaks, and the high frequency components can easily be eliminated with an anti-alias filter.

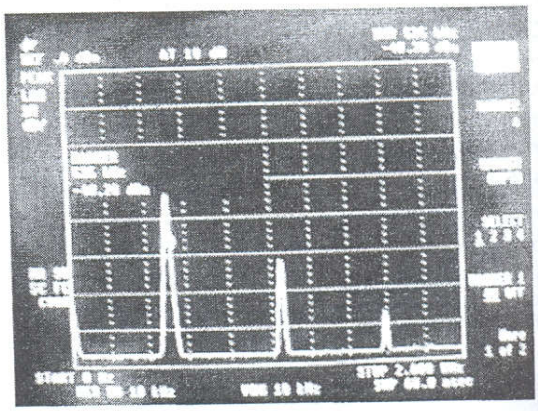

Figure 4. Signal Spectrum

Digital parts of AD-converters can also be integrated on FPGA. As mentioned, Xilinx also offers delta-sigma AD-converters. These converters however are very limited in performance, wherefore an alternative approach was investigated in order to achieve a higher performance. For this purpose a successive approximation algorithm was implemented in VHDL for Xilinx FPGAs. With this algorithm, digital words of 12 bits are generated and written on the FPGA output pins. These digital words can be converted into an analogue signal by using a simple R2R converter.

In order to further optimize the power consumption, dynamic clock scaling has been integrated on FPGA.

Clock scaling is a standard technique in microcontroller based systems in order to reduce the dynamic energy consumption by putting the microcontroller in different activity modus. To implement this in FPGA based systems is not as straight forward, due to the structure of the FPGA clock network.

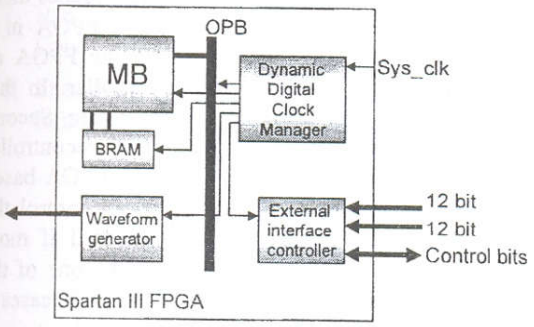

Figure 5. System Overview

Clock scaling was integrated in a FPGA based system for a signal processing application, by designing a core in VHDL for dynamically adjusting the clock frequencies, see Figure 5 for a system overview. The system uses a soft-core MicroBlaze microcontroller for executing the data processing, but also includes additional peripherals such as the sinus generator and a user defined IP core for reading data from external AD-converters. The system starts collecting the data and processing them every 100 ms. As soon as the data has been processed, the MicroBlaze core can be put into sleep modus. Also, the other components can be put into sleep modus as soon as the MicroBlaze has collected the data and started processing them.

The dynamic power consumption was estimated with available FPGA tools with and without integrated clock scaling. The results of the different dynamic power consumptions are shown in Table 0.

Table 2. Dynamic Power Consumption

	Dynamic Power Consumption
Without clock scaling	24.94 mW
With clock scaling	9.87 mW

The results show that the dynamic power consumption was reduced approx. 60% by integrating clock scaling. Using this technique in FPGA based systems is a requirement for designing self-adaptive systems that can adjust the clock frequencies dynamically according to the workload.

5. Future Trends of Ad-Hoc Sensor Networks

Wireless-Sensor-Networks usually consist of a very high number of nodes. In large networks there can be several thousands nodes that make controlling the network manually impossible. Therefore new approaches are needed for configuring, organizing and controlling such a network and its behaviour. Organizing all these nodes requires high sophisticated methods that have to be implemented.

Almost all ad-hoc wireless sensor networks use hop to hop communication due to the very small communication range. Therefore routing algorithms are needed that can benefit from localization algorithms that detect the position of a node. In the routing manner a relative localization is fully sufficient. That means no absolute position is detected. But also for the collection of physical sensor data the information about a nodes position is very useful. In some cases only the combination of measured data and measurement position will make sense. Requesting information can also be supported by localization algorithms. Assuming an area with a high density of sensor nodes it can be sufficient to get the data from a very few number of these sensor nodes. The other nodes can remain inactive. It has also to be taken into account that in many cases the absolute and relative position of the nodes is not fixed within the network. Therefore localization is a task that has to be run from time to time to get the structure of the network.

Another important point is data encryption. In Networks that are measuring human related or other confidential information encryption maybe an interesting issue. Normally there is no possibility to ensure the overall security of a network. The very high number of sensor nodes and the large area they may be distributed at makes it also almost impossible to prevent the network from attacks or spying. The only way to solve the problem is to encrypt any or selected information that is send over the network.

It's easy to see, that the two mentioned services, localization as well as encryption, maybe very useful in many Wireless Sensor Actuator Networks.

Unfortunately both mentioned algorithms need a huge amount of computing power that exceeds the possibilities of Microcontrollers like the MSP430, which is one of the most common devices in sensor networks. Bringing in high performance microcontrollers or even DSPs can solve the computing power problem. On the other hand these devices need much more energy than the MSP430. The usage of the powerful devices would lead to a very short operation time and is therefore not possible.

The utilization of reconfigurable hardware that has already been introduced in chapter 4 may solve the problem. One of the companies investigating reconfigurable hardware in sensor node is Intel [13]. But currently there is only few effort spent in investigating the usage of FPGA technology for sensor nodes due to several reasons. This is mainly related to energy consumption of these devices. Regarding this point newer devices consume less power than former versions. There are different device classes available on the market that are suitable for different applications and differ in size

and features. One of the main differences in the context of power consumption is the type of configuration. Most of the FPGAs use SRAM based configuration memory that needs to be configured on Powerup of the system. This takes time and energy that can be saved by using FPGAs using flash based configuration memory. These devices have less leakage current and therefore manage to work with less energy. Another advantage is the power up where no configuration has to be loaded. Time and energy can be saved. There are also devices that need even less energy compared to the flash based solution. One Time Programmable (OTP) FPGAs use the Fuse or Antifuse technology to store the configuration inside the chip but have the disadvantage to be inflexible. There is no possibility of an update in the field or the application of much more advanced methods.

Nevertheless in most cases FPGAs will use more energy compared to the MSP430 microprocessor while being much more flexible and powerful. Using FPGAs as ASIC replacement could lead to the wrong conclusion that especially SRAM based FPGAs do not suit to any sensor network due to their power consumption. In fact there are several reasons why reconfigurable techniques are also very interesting for sensor networks. Regarding power consumption there are many methods that help saving power. Using the flexibility of FPGAs it is possible to parallelize and pipeline the algorithms running on an FPGA in a very high degree. On one side that makes the algorithms very efficient and fast and allows on the other side to scale system frequency down and therefore reduce power consumption. Energy consumption can further be reduced by using clock scaling and clock gating techniques that have been described in chapter 4. Moreover it is quite likely that the algorithms are not needed all the time. Then energy can be saved with clock scaling. The localization as well as the encryption algorithm are normally idle most of the time and so the clock can be turned off.

Usually all the algorithms are implemented on the FPGA in parallel and also run in parallel. Such an implementation of all needed algorithms in parallel may use a lot of resources. To decrease the size of the design also reduces the size of the needed FPGA. A smaller device has less power consumption. So shrinking the design size is one of the most challenging tasks. This can not only be done statically. Some FPGAs support the partial reconfiguration of the device. That means only a small portion is reconfigured while the other regions remain active. That makes it possible to use the same area for several different functions that are not needed at the same time. The use of partial reconfiguration enables the user to change the behaviour of the FPGA and thus the behaviour of the whole node. Picking up the two algorithm examples from above Localization and Encryption maybe not needed at the same time and could share the logic resources. Whenever the next function is needed it is loaded from an external memory and configured into the FPGA. This can also be done by the FPGA itself. The possibility of partial and dynamic reconfiguration makes the utilization of very small FPGA devices possible that can be added to every sensor node in the network. This enables all nodes to adapt more flexible to any changes in the network topology or environment.

For realizing the described methods and approaches there are generally two possibilities for using a FPGA in a sensor node. The first version is to use the FPGA as standalone replacement for the microcontroller. In this case it is quit likely to add a Softcore Processor. Second version is to use a MSP430 or another microcontroller based solution which is supplemented by a FPGA based co processing unit. Then the MSP430 can control the sensor node and the FPGA is only activated if more computational power is needed. This will be one of the further extensions of the Zigtiv Mote. In both cases a solution that includes FPGAs enables the application of high sophisticated algorithms that are used i.e. for localization or encryption.

6. Conclusions

This paper presents the realization of low power sensor nodes for health care applications as well as alternative hardware architectures for ad-hoc sensor networks.

Future hardware/software architectures in wireless sensor networks are likely to be heterogeneous in terms of granularity and performance. For example, a sensor node can integrate a mixture of components such as a microcontroller and fine/coarse granular reconfigurable hardware. This will enable a dynamically optimized hardware topology for the specific sensor network application. By exploiting the run-time configuration the architecture and the network can adapt to unpredictable scenarios of the environment and thereby provide a high degree of flexibility for system integration.

Acknowledgments

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The KineMedic Robot - Introducing Soft Robotics into the OR

T. Ortmaier
German Aerospace Center
Institute of Robotics and Mechatronics
Wessling, Germany
e-mail: Tobias.Ortmaier@dlr.de

Abstract[1]

The paper is concerned to the KineMedic robot and its introducing into the operating room.

1. The Main Results

Many attempts have been made to introduce mechatronic assistance systems into the operating room (OR) recently. Crucial for their acceptance by the surgeon are both an intuitive, easy to use man-machine-interface and an appropriate level of autonomy. For advanced mechatronic systems soft-robotics seems to be a suitable approach to combine haptic man-machine introduction and autonomy: the surgeon is able to move the robot by touching its structure and pulling/pushing it towards the desired pose. At the same time the motion can be restricted by virtual fixtures preventing the surgeon e.g. to damage delicate structures unintentionally or allowing him to move the tool-tip along a predefined trajectory. Thus the strengths of human and robot can be combined: the surgeon is able to utilize qualitative information whereas the robot provides high accuracy and various control schemes.

This presentation introduces the KineMedic robot which was developed at the Institute of Robotics and Mechatronics of the German Aerospace Center. The light-weight and kinematically redundant robot was optimized for the usage in the crowded and unpredictable OR. Thanks to the torque sensors integrated into the robot joints and the implemented control schemes the measurement of forces applied to the robot structure is possible, enabling the before mentioned soft-robotics concept. In this talk the basic ideas, the robot hardware, as well as the control laws are presented. Additionally first medical applications including biopsy and the placement of pedicle screws are shown.

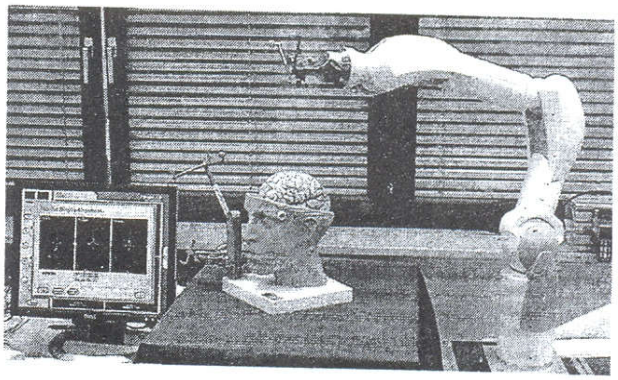

Figure 1. The KineMedic Robot in Biopsy Application

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