Development, Realization and Research Ternary Arithmetic and Logic Units in Ternary Bases

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Abstract[1]

The object of the article is ternary bases research by development and realization of ternary arithmetical-logic units in some bases. The developed arithmetical-logic units were realized and simulated with binary coded model.

1. Introduction

The interest associated with ternary logic and arithmetic has appeared long before first computers occurrence because of symmetric code especial properties.

The main ternary code advantage over the binary code accepted in contemporary computers is ternary code profitability.

The comparison of ternary code basic characteristics defining ternary code and the three-value logic practical value with a same in binary code is listed below:

- number with a sign natural presentation;
- number sign is defined by a senior nonzero digit sign;
- simple numbers comparison;
- branching command on a sign occupies twice less time;
- correct rounding at number length truncation;
- subtraction is replaced by addition with the inverted item;
- ternary counter is reversible automatically;
- carry to the following position in the three-input ternary summator appears in 8 case of 27, but in the binary summator – in 4 of 8;
- multiplication and division table simplicity in ternary notation is the same as in the binary;
- three-level signal more stability to noise influence in transfer lines.

2. Ternary devices realization and modeling

Three-value logic elements hardware realization can be considered from two positions. The first approach – ternary functions modeling with binary coded model [1]. In this presentation one trit occupies two bits and one more level remains uncertain. It can be used for a dividing comma in numbers designation or high-impedance conditions on an exit indication. Binary modeling is caused by accessible three-level elements absence and the standard binary one use instead of them. The second approach of three-level devices realization is associated with essentially new logic element with three states development [2].Ternary arithmetic-logic units' realization, modeling and research were accomplished with the first approach use on the field-programmable gate array (FPGA) and Computer-Aided Design Xilinx and were fulfilled at the stand with S10PC84 FPGA use.

3. Ternary memory cell and ternary triggers

The problem of trigger schemes construction on the basis of ternary logic elements is existed.

In the binary logic all trigger schemes structures use the elementary storage element – memory cell.

The memory cell in the binary logic is the scheme having two inputs: S (Set) and R (Reset) and two outputs Q and notQ. The resolved outputs states are only opposite states (0, 1) or (1, 0). The switching signal on S-input establishes memory cell in a state 1 (Q = 1, notQ = 0), and on R-input - in a state 0 (Q = 0, notQ = 1). Usually memory cell consists of two logic elements which are mutually captured by a feedback.

It is possible to assume that in the ternary logic there should be a similar memory cell (ternary storage element) too.

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Thus, ternary memory cell is a storage element of trit, designating information unit in the ternary logic (-1, 0 and 1 or 0, 1 and 2).

As three various values exist in the ternary logic, ternary memory cell should have three outputs 1Q, 2Q, 3Q with three various states (by analogy to exits Q and notQ at the binary trigger).

The resolved ternary memory cell output states are the following: (1Q, 2Q, 3Q) = (0, 1, 2), (1, 2, 0) and (2, 0, 1). Ternary memory cell realization in Vebb basis is shown on Fig. 1. The Vebb function truth table is shown on Fig. 2.

a	*b*		
	0	**1**	**2**
0	1	2	0
1	2	2	0
2	0	0	0

Fig. 1. Vebb function truth table

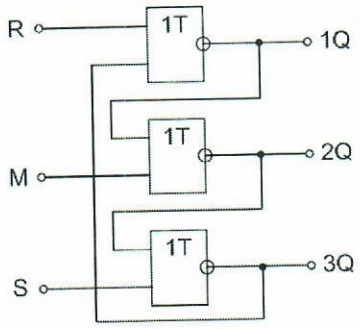

Fig. 2. Ternary memory cell

The implemented thorough research of the developed ternary memory cell structure and the received transitions table consideration have allowed to make a number of following important conclusions concerning offered structure ternary memory cell properties.

The inputs state (R, M, S) = (0, 0, 0) provides any ternary memory cell state storage.

Switching from any current state in one other state is realized by change from 0 to 2 one of inputs:

- on R-input ternary memory cell switches in a state (0, 1, 2),
- on S-input ternary memory cell switches in a state (1, 2, 0),
- on M-input ternary memory cell switches in a state (2, 0, 1).

4. The arithmetic-logic unit characteristics

The ternary arithmetic-logic unit with certain parameters in various ternary bases has been decided to realize and investigate for ternary bases research from the designing and realization simplicity, developed realizations bulkiness and a transparency, spent figurative elements quantity, developed ternary digital complexity and speed devices points of view.

The realized ternary arithmetic-logic units have the following operations set:

- multiplication,
- addition,
- subtraction.

The ternary arithmetic-logic units' whole ternary numbers digit capacity is equal 3.

5. Conclusions

Ternary arithmetic-logic units' realization was accomplished in Rosser and Turquette basis and Vebb basis. In the issue of arithmetic-logic unit implementation, modeling and research were received the following results. Rosser and Turquette Basis is more simple, evident and transparent for ternary digital devices construction. The Vebb basis is single-element basis. Similarly single-element bases prevalence in the binary logic, it is enough to have only the same ternary elements realizing Vebb function for ternary digital devices construction.

Also the technique of the ternary digital devices realization in Vebb basis has been developed for the question decision of a basis choice in the three-value logic and a base ternary elements set preferable to digital systems realization in the ternary logic.

The full system of ternary functions in non-classical logic basis, in the modular logic, and Vebb basis has been realized on the basis of base elements Xilinx FPGA.

Known algorithms have been studied, and also new any figurative functions realization algorithms with use of the created ternary elements sets are developed, including for the first time the developed any ternary functions presentation and simplification in Vebb basis algorithm.

Also the memory cells construction question in Vebb basis on which basis, difficult digital devices with memory in this basis synthesis and realization questions are studied and described has been investigated. Within this section limits the ternary memory cell structure construction decision with which use it is possible to synthesize any ternary trigger schemes and digital elements with memory for the first time is offered.

Further research of the Post basis and the modular logic basis are planned.

References

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